In re Appln. of Nick P. DiVittorio
Application No. 09/449,912

REMARKS

The Office Action dated December 19, 2003, and the references cited therein have been carefully considered. Claims 1-26 are presently pending. No claims currently stand allowed. None of the claims have been amended. In view of the remarks set forth herein below, the pending claims 1-26 are patentable over the prior art presently known to Applicant. Accordingly, Applicant requests favorable reconsideration of the previous rejection of the now pending claims. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of the Claim Rejections

The following identifies the authority and prior art applied to the identified claims for each objection and/or rejection of the claims set forth in the Office Action dated March 20, 2003.

1. **Section 2:** The drawings are objected to under 37 C.F.R. 1.83(a) because the drawings do not specifically show "first configurable repetition period" (claim 26), "PID block" (claims 6 and 18) and "ratio block" (claims 7 and 19).

2. **Sections 3-7:** Claims 1-2, 5, 13-14, 17 and 25 are rejected under Section 103(a) as obvious over Dailey U.S. Pat. No. 6,330,483 (filed May 7, 1999 and issued Dec. 11, 2001) in view of Daggett et al. U.S. Pat. No. 4,786,847.

3. **Sections 8-9:** Claims 3-4 and 15-16 are rejected under Section 103(a) as obvious over Dailey in view of Daggett et al. and Morshedi et al. U.S. Pat. No. 5,481,716.

4. **Sections 10-19:** Claims 6, 8-12, and 20-24 are rejected under Section 103(a) as obvious over Dailey in view of Daggett et al. and McManus et al. U.S. Pat. No. 4,788,647.

5. **Section 20:** Claims 7 and 19 are rejected under Section 103(a) as obvious over the Dailey in view of Daggett et al. and Westergren et al. U.S. Pat. No. 5,423,076.

6. **Section 21:** Claim 26 is rejected under Section 102(e) as obvious over Dailey in view of Wright et al. U.S. Pat. No. 6,101,599.

Applicant traverses the grounds for each and every rejection for the reasons set forth herein below.

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Attention is initially directed to the objections in **section 2** to the drawings as not showing particular recited claim features "first configurable repetition period" (claim 26), "PID block" (claims 6 and 18) and "ratio block" (claims 7 and 19). The PID and Ratio blocks are identified by reference number "130" in FIG. 3 of the drawings. The "first configurable repetition period" – recited in claim 26 – corresponds to the embedded application cycle referenced by, for example, decision block 302 that identifies the "Embedded App. Cycle Period." The corresponding written description a pages 15-16 states:

> The embedded multivariable control application 138, like the control blocks, has a **user-configurable cycle period** defining the refresh period for the embedded control application 138. ...
>
> If at step 302 the MVC block determines that the configured cycle period has expired, then control passes to step 304 wherein the MVC block 136 determines whether the embedded multivariable control application 138 is still busy (i.e., an iteration of the embedded multivariable control application task is not completed for the previous configured embedded application cycle period).

Thus, Applicant respectfully submits that the claimed features are adequately represented in the drawings and amendments to the drawings are not required to comply with 37 C.F.R. 1.83. However, Applicant is amenable to any modifications suggested in any subsequent office actions.

Applicant traverses the rejection, at **sections 3-7** of the Office action, of claims 1-2, 5, 13-14, 17 and 25 under Section 103(a) as obvious over Dailey in view of Daggett et al. U.S. Pat. No. 4,786,847. As an initial matter, in responding to this Office Action, Applicant again explicitly reserves the right (and stands ready if necessary) to swear behind the Dailey reference – and thereby eliminate it as a reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not, in combination with the Daggett et al. '847 patent, render Applicant's claims obvious.

Applicant traverses the rejection of **claim 1** at **section 3** of the Office Action. Claim 1 recites a control processor (a single piece of computing hardware on a network – see control processor 2 in Fig. 1, and control processor 102 in Figs. 2 and 3) that, in addition to executing a set of control blocks at a relatively high execution priority status (according to well-known control processor architectures), executes *a specific type of process control program at a relatively low execution priority status*. The relatively low execution priority status process

control program is referred to in claim 1 as an embedded control task (referred to as an "embedded control application 138" in the written description). The embedded control task/application comprises a multivariable linear program that establishes process setpoints. The set of control blocks (assigned the relatively high execution priority status) drive a set of output signals controlling a set of field devices associated with the industrial process. The two distinct classes of program sequences recited in claim 1 are *executed* at distinct *execution* priority status levels in order to implement the dynamic model-based interactive control of the industrial process recited in the preamble.

The Dailey patent, upon which the rejection of claim 1 is primarily based, discloses a flight control system for a flying object (e.g., an airplane, rocket, missile, etc.). The Dailey patent discloses a control system including potentially multiple command channels – the output signals that control rudder, aileron, flap, etc. positions on the flying object. The Dailey patent first discloses a way for eliminating integrator windup (when a controlled element cannot change as quickly as desired by the control system). The Dailey patent also discloses a control method including assigning priorities to *output channel values* governing how the values are applied to flight surface actuators for controlling flight – in other words, Dailey applies a priority to how calculated output channel values are *applied* to flight surface control elements. Nowhere does Dailey suggest that the differing control signal channel priorities are in any way linked to *execution* priority of code sequences associated with the signal channels.

In contrast to program sequence execution status, Dailey's reference to "priorities" concerns, as explained at col. 18, lines 22-41, control affecters. The primary control affecters are used first, then the secondary control affecters are used when the primary control affecters saturate. This teaching is reinforced at column 19, lines 46-64. Thus, Dailey discloses prioritization of control affecters (output channels) rather than prioritizing execution of the two distinct sets of cyclically executing program sequences described in claim 1. With regard to Applicant's position regarding the use of "priority" in Dailey, it is further noted that Dailey also appears to disclose a single cyclically executed control loop that calculates both the primary and secondary channel values. Dailey, at col. 39, lines 1-3 refers to beginning a new iteration cycle. Thus, for each iteration cycle, the controller calculates new values for all channels (both primary and secondary) – regardless of the channel's priority.

Dailey discloses foreground/background calculation of the *same control values* (at column 37, lines 20-28) that are output to control elements for flight control surfaces directing the path of a flying object. Applicant notes, however, the recited invention in claim 1 is not merely directed to the presence of multiple execution levels in a computer system. Rather, the invention recited in claim 1 embodies merging and prioritizing execution of two functionally distinct industrial process control system tasks within a single control processor. The recited control processor in claim 1 executes: (1) a model-based multivariable linear program providing process setpoints that is executed at a relatively low execution priority; and (2) a set of control blocks that are executed at a relatively high execution priority and have output values that are transmitted to field devices controlling operation of the industrial process.

With regard to the Daggett reference, Applicant does not contest that control blocks have been previously executed, on a relatively higher priority basis, in the past within a control processor. However, modifying Dailey in view of Daggett does not disclose a combination within a control processor that includes the recited embedded control task. *If anything, such combination merely teaches rendering flight control channel values via program sequences executed at a high priority level.* Thus, the combined teachings of Dailey and Daggett based upon the ordinary skill in the art at the time of the invention does not render a combination including each of the features/characteristics of the recited embedded control task.

Turning to the "Response to Arguments" beginning at page 18 of the Office Action, Applicant initially notes that in the responses, the Office Action does not address Applicant's contention (at page 12, lines 14-18 of the previous Office Action response) that Dailey neither discloses nor suggests implementing the disclosed flight surface control system using *control blocks*. In order to determine the merits of the Office Action's assertions regarding the teachings of Dailey, Applicant respectfully requests identification (preferably by reciting a drawing reference number) of the components within Dailey that correspond to the recited set of control blocks. Similarly, Applicant requests specific identification of the distinctly claimed "embedded control task" and the process setpoints provided by the embedded control task.

Furthermore, contrary to the Office Action's argument at section 24, Dailey's channel priority does not meet the "execution priority" aspect of the invention recited in claim 1. In response to Applicant explaining that Dailey's teachings regarding prioritizing channels refer to *applying* values assigned to channels – not execution precedence of control program sequences that render the channel values –, the Office Action, at section 24, states that a suggestion to combine the Dailey and Daggett references arises from the knowledge generally available to one of ordinary skill in the art. However, the Office Action's response appears to miss Applicant's point that Dailey's "channel priorities" have nothing whatsoever to do with preempting execution of lower priority program sequences to execute higher priority program sequences. The Dailey reference, after acknowledging the difficulty/challenges of coordinating control of non-instantaneous control elements of an aircraft in response to sudden, large, changes in control surface inputs (see, col. 2 of Dailey), proposes a prioritization scheme that assigns differing priorities (primary/secondary) when *applying* the channel values to the control surface elements to maintain the stability of the flight control system while transitioning to a new flight control surface state. Nowhere does Dailey disclose or suggest that the priorities assigned to the channels in any way relate to preferential *execution of control program sequences* (control blocks) relating to those channels. In the event that this rejection is not withdrawn, Applicant specifically requests identification of where Dailey teaches *multi-level program sequence execution* wherein certain program sequences are executed at a lower execution priority status based upon channel priorities. It is further noted by Applicant that all of the control surface channels appear to be processed at a same *execution priority status* regardless of their assigned priority.

In response to Applicant's traversal of the Office Action's rejection of claim 1 for failure to disclose the embedded control task and the set of control blocks being executed according to differing execution priority status levels in a single control processor, the current Office Action, at page 4, takes "Official Notice" that placing tasks on a single processor is well known. Applicant does not disagree with such assertion. However, contrary to the Office Action's assertion at section 24, even assuming that executing multiple tasks on a single processor is well known, the Dailey reference does not disclose the claimed combination of elements recited in claim 1 that specify *two functionally-distinct types of control program components executed according to differing execution priority status levels* in a single control processor. Instead,

Daily discloses a set of channels assigned to a same *execution* priority status, but having differing priority when *applying* the output values to actual control elements.

Contrary to the Office Action's assertion at section 25, Dailey neither discloses nor suggests a background task, *executed at a relatively low execution priority status*, renders process setpoints in a control processor that executes a set of control blocks, including regulatory control blocks, that are executed at a relatively higher execution priority status. The Office Action's response to Applicant's argument does not identify where the alleged teachings are provided in Dailey. In the event that this rejection is not withdrawn Applicant respectfully requests identification of where the Dailey reference discloses the recited embedded control task (comprising a multi-variable linear program) *executing at a relatively low priority on a control processor that provides process setpoint* output values.

Applicant respectfully submits that the Office Action has not demonstrated that the invention recited in claim 1 is obvious since one of ordinary skill in the art would not have been motivated by the teachings of the prior art to modify the flight control system of Dailey in view of Daggett to render the recited invention. Addressing the Office Action's response at section 26, the cited text from Applicant's remarks is a *conclusion* that summarizes Applicant's primary argument – the basis of which is stated in the paragraphs preceding the conclusion. Simply put, Applicant submits that placing the two functionally distinct identified types of process control program sequences in a single control processor and *executing* the two types at relatively low and relatively high execution priority statuses is neither disclosed nor suggested by the cited combination of references.

For at least the above reasons, Applicant traverses the rejection of **claim 13** at **section 6** of the Office Action. Though the claimed method differs from claim 1 in a number of ways, including the recitation of receiving (rather than transmitting) process variables, the claimed invention is similarly distinguished over the prior art teachings by the presence of the merged execution, on a single control processor, of functionally distinct and specifically identified process control program components at different execution priority levels. An embedded multivariable control application is executed at a lower priority level to supply setpoint values corresponding to a process control variable (that in turn effects a regulatory

control block), and a set of regulatory control blocks are executed at the relatively higher level.

Applicant acknowledges the additional comments in the most recent Office Action taking "Official Notice" with regard to executing multiple tasks on a single processor. However, as explained in considerable detail above, the present invention recites specific tasks executed at two distinct levels of execution priority (e.g., foreground/background). If the rejection of claim 13 is not withdrawn, Applicant requests specific identification of each of these two distinct types of control system software sequences within a single control processor – and/or the suggestion to modify a prior art industrial process control processor to include these two specific types of software executed at differing priority levels.

Applicant traverses the continued rejection of **claims 2 and 14 in section 4** of the Office Action. Claims 2 and 14 depend from and include all the recited elements of claims 1 and 13, respectively. Thus, for at least the reasons set forth above for claims 1 and 13, claims 2 and 14 are patentable over the prior art.

Applicant previously stated that in contrast to the "supervisory control blocks" recited in claims 2 and 14, the "supervisory control" discussed within the Daggett reference concerns a second computer (connected via a local area network) and thus does not meet the requirement of being executed within the control processor. Furthermore, "Supervisory program execution" (in Daggett) to the extent understood by Applicant, does not refer to the recited "supervisory control blocks" that execute within the control processor. Applicant further traverses the rejection of claims 2 and 14 since there is no suggestion to incorporate the regulatory/supervisory control block-based process control system architecture recited in claims 2 and 14 into the flight control system described in Dailey – that makes no reference whatsoever to control blocks. *In the event that the rejection is not withdrawn, Applicant requests an explanation of how "supervisory control" and "supervisory program execution" disclose Applicant's recited "supervisory control blocks" that are described in the specification as time-critical, higher level (i.e., supervisory) control blocks that are distinguished from low level regulatory control blocks.*

Applicant traverses the continued rejection of **claims 5 and 17 in section 5** of the Office Action. Claims 5 and 17 depend from and include all the recited elements of claims 2 and 14, respectively. Thus, for at least the reasons set forth above for claims 1, 2, 13 and 14, claims 5 and 17 are patentable over the prior art.

Applicant previously stated that the matrices disclosed in the Dailey patent do not constitute a multivariable loop (MVL) block. The specification describes the MVL block at page 9 of the specification as follows:

> A multivariable loop (MVL) block 132 applies input variable values obtained from a number of sources to a control equation/program incorporated within the MVL block 132 to render a manipulated variable (MV) supervisory set point that is written to the regulatory control block 130. In the exemplary embodiment of a multivariable controller embedded within a control processor, the MVL block 132 receives as its inputs a setpoint value (generated by the embedded linear programming optimizer, by a non-embedded supervisory control program, or manually entered by a process operator) , a controlled variable (CV) from the input block 126, and a feedforward variable (FV) from the input block 128.

In the event that this rejection is not withdrawn, Applicant requests an explanation of how the matrices described in Dailey constitute the MVL block that, as defined in the specification and recited in claims 5 and 17, *supplies an input value to a regulatory control block.*

Applicant traverses the rejection of **claim 25 in section 7** of the Office Action. Claim 25 is similar to the other rejected independent claims. However, the recited functions associated with the relatively low and high execution priorities differ from the functions recited in claim 1. Claim 25 recites an industrial process control computer including multiple operating levels. At a background (interruptible, lower priority) level, the process control computer executes a multivariable process control application that includes instructions for implementing a multivariable linear program that generates a set of values *corresponding to process control variable* setpoints. At a foreground (interrupt driven, higher priority) execution level, the process control computer executes a set of control blocks. The set of control blocks include program instructions for *receiving and storing a set of process variable values representing the state of a controlled process.*

A number of elements of claim 25 have been distinguished from Dailey herein above, and those comments (e.g., distinguishing signal channel priorities and program sequence execution priority) are incorporated by reference. Dailey does not disclose or suggest a "control block" based control system. Furthermore, there is no suggestion in either Dailey or Daggett that such control blocks can/should be used to carry out the flight control system described in Dailey.

Applicant acknowledges the most recent Office Action taking "Official Notice" with regard to executing multiple tasks on a single processor. However, as explained in considerable detail above, the present invention recites two functionally distinct types of tasks executed at two distinct levels of execution priority (foreground/background). *If the rejection of claim 25 is not withdrawn, Applicant requests specific identification of each of these two distinct types of control system software sequences within a single control processor – and/or the suggestion to modify a prior art industrial process control processor to include these two specific types of software executed at differing priority levels.*

As previously explained by Applicant, neither Dailey nor Daggett suggest the execution of a multivariable linear program and control blocks at specified background and foreground program sequence execution levels within a single process control computer as recited in claim 25. Dailey, at column 37, lines 20-28, does recite foreground/background execution of control calculations. However, Dailey does not teach or suggest that a multivariable process control application, executed in the background, renders process control variable setpoints, and that a set of control blocks execute in the foreground to receive and store process variable values representing the state of the controlled process. In the event that the rejection of claim 25 is not withdrawn, Applicant requests specific identification of these differing types of instruction sequences/process control constructs within the cited references as well as the suggestion to combine the teachings of Dailey and Daggett to render such a combination.

Contrary to the Office Action's assertion at section 25, Dailey neither discloses nor suggests an embedded multivariable process control application executes as a background task that renders *process control variable* setpoints in a control processor that executes a set of control blocks, including a set of control blocks that receive and store a set of process variable values, at a relatively higher execution priority status. The Office Action's response

to Applicant's argument does not identify where the alleged teachings are provided in Dailey. In the event that this rejection is not withdrawn Applicant respectfully requests identification of where the Dailey reference discloses an industrial process control computer having the recited embedded multivariable process control application (comprising a multi-variable linear program) *executing at a background control program execution level on a control processor* that generates values corresponding to process control variable setpoints.

Applicant continues to traverse the rejection of **claims 3-4 and 15-16 in sections 8-9** of the Office Action as obvious over Dailey in view of Daggett et al. and Morshedi et al. U.S. Pat. No. 5,481,716. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference – and thereby eliminate it as a reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not, in combination with the other cited references, render Applicant's claims unpatentable since Dailey and the other cited references, as explained previously herein above, lack a number of the recited elements in the claims from which claims 3-4 and 15-16 depend.

Applicant traverses the rejection of **claims 3 and 15 in section 8** of the Office Action. Claims 3 and 15 depend from and include all the recited elements of claims 2 and 14, respectively. Thus, for at least the reasons set forth above for claims 1, 2, 13 and 14, claims 3 and 15 are patentable over the prior art.

Furthermore, claims 3 and 15, include the further element/step of a multivariable *control* (MVC) block (see, e.g., MVC block 136) that facilitates communicating data between the control processor and a workstation. This special purpose high execution priority block controls/manages the operation of various other components in the control processor 102. Claim 15 calls for downloading the data from the workstation to a database accessed by the MVC that executes on the control processor.

As an initial matter, Applicant notes *none* of the cited references discloses the MVC block (described at page 9 of Applicant's specification in association with MVC block 136 of FIG. 3). Furthermore (with regard to claim 15), nowhere does Dailey suggest that its flight control system receives data (placed in a database), from a workstation, that is accessed by a

multivariable control block – or the desirability/benefits of adding the particular described workstation/process controller data interface to the flight control system. *In the event that the rejection of claims 3 and 15 is not withdrawn, Applicant again requests identification of the MVC block in Dailey (if such exists) as well as the suggestion to modify Dailey's flight controller to include the recited functionality in claims 3 and 15.*

Responding to the Office Action's response at section 27, Applicants agree that control blocks are well known in the context of control processors. However, claims 3 and 15 specify a specific type of control block (MVC) that is executed at a high priority on the control processor to perform a variety of functions for controlling components of the control processor that is neither disclosed nor suggested in the cited references.

Applicant traverses the rejection of **claims 4 and 16** in **section 9** of the Office Action. Claims 4 and 16 depend from and include all the recited elements of claims 3 and 15, respectively. Thus for at least the reasons set forth above for claims 1-3 and 13-15, claims 4 and 16 are patentable over the prior art.

Furthermore, claims 4 and 16 additionally recite the element/step of the MVC block receiving/storing a process control model that is implemented by the embedded control task/control application. Nowhere in the cited portions of the Dailey reference is this element/step described. In fact, there is no description of how the matrices are populated in the Dailey flight controller. On the other hand, one would expect the flight control model to be highly stable and not likely to be changed (for reasons of safety). Thus, one would not expect Dailey's flight controller to support the claimed functionality recited in claims 4 and 16 that enhance the alterability of a previously loaded control model while the control system is operating. For at least these reasons, there is no suggestion to create the inventions recited in claims 4 and 16. *In the event that this rejection is not withdrawn, Applicant requests identification of a teaching in the prior art to make such modifications to the cited prior art flight control system to render the claimed invention.*

Responding to the Office Action's response at section 27, Applicant agrees that control blocks are well known in the context of control processors. However, claims 4 and 16 specify a specific additional function performed by the MVC recited in claims 3 and 15 that is neither disclosed nor suggested in the cited references.

Applicant traverses the rejection, in **sections 10-19** of the Office Action, of **claims 6, 8-12, and 20-24** under Section 103(a) as obvious over Dailey in view of Daggett et al. and McManus et al. U.S. Pat. No. 4,788,647. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference – and thereby eliminate it as a reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not render Applicant's claims unpatentable since Dailey and the other cited references, as explained previously herein above, lack a number of the recited features of the claims from which claims 6, 8-12 and 20-24 depend.

Applicant traverses the rejection of **claims 6 and 18** in **section 10** of the Office Action. Claims 6 and 18 depend from, and include the elements of, claims 5 and 17. Thus, for at least the reasons set forth above for claims 1, 2, 5, 13, 14 and 17, claims 6 and 18 are patentable over the prior art. Claims 6 and 18 recite the additional element/step of a PID block. Though Applicant agrees that McManus discloses a PID block, Applicant asserts that the modification asserted by the Office Action is neither suggested nor desirable in Dailey's flight controller. *In fact, the disclosure/invention described in Dailey appears to take the place of a PID control block.* Thus, there is no suggestion to modify the Dailey flight controller to include a PID control block. In the event this rejection is not withdrawn, Applicant requests an explanation of why (and how) one skilled in the art would be motivated to modify the flight controller disclosed in Dailey to *specifically* include the recited PID control block.

Responding to the Office Action's response at section 27, Applicant agrees that control blocks are generally well known in the context of control processors. However, claims 6 and 18 specify a specific type of control block that, while well known, is conspicuously not present in the Dailey reference. If the rejection is not withdrawn Applicant requests citation to the prior art suggesting the incorporation of a PID control block into the system disclosed in Dailey.

Applicant traverses the rejection of **claim 8** in **section 11** of the Office Action. Claim 8 depends from, and includes all the elements of, claim 1. Thus, for at least the reasons set

forth above for claim 1, claim 8 is patentable over the prior art. Claim 8 recites a repetition cycle parameter that specifies a repetition period for the embedded control task recited in claim 1. Claim 8 further defines the industrial control processor architecture recited in claim 1 by adding an element of configurability to the repetition period of the embedded control task. The McManus reference discloses a configurable repetition period for a "power calculation task." The Office Action does not assert that this power calculation task has anything to do with the claimed "embedded control task" nor does the Office Action identify where, in the cited references, teachings suggest that such a configurable parameter should be incorporated into the Dailey control system. Such a modification to Dailey cannot be suggested by the McManus reference since the embedded control task does not even exist in Dailey.

In summary, the Office Action asserts, but does not explain where the prior art suggests modifying the Dailey flight controller to include an embedded control task (executing at a lower execution priority) having a configurable repetition period. However, the Dailey reference does not even disclose the embedded control task and the configurable repetition period in McManus merely relates to a power calculation task. *Applicant again requests identification of the above-identified deficiencies in the teachings/disclosure in the prior art in the event that the rejection of claim 8 is not withdrawn.*

Applicant traverses the rejection of **claim 9** in **section 12** of the Office Action. Claim 9 depends from, and includes all the elements of, claim 8. Thus, for at least the reasons set forth above for claims 1 and 8, claim 9 is patentable over the prior art. Claim 9 recites the additional element of a supervisory control block that controls restarting a repetition cycle of the embedded task in accordance with the repetition period parameter. While McManus, by necessity, includes some form of scheduling entity that controls the repeated "power calculation task," *nowhere does McManus disclose that this function is carried out by a supervisory control block that executes within the control processor.* In the event that the rejection is not withdrawn, Applicant requests identification of disclosure in the prior art suggesting the specifically recited program execution control/management arrangement.

Applicant traverses the rejection of **claim 10** in **section 13** of the Office Action. Claim 10 depends from, and includes all the elements of, claim 1. Thus, for at least the reasons set forth above for claim 1, claim 10 is patentable over the prior art. Claim 10 recites the additional element of a block processing cycle parameter that specifies a repetition period for executing the set of control blocks. The prior art however, fails to suggest modification of the Dailey reference (which does not even disclose control blocks) to include a parameter designating a block execution cycle repetition period.

Applicant, as an initial matter, traverses the assertion in the Office Action that every control system, by necessity includes control blocks. Many control systems do indeed incorporate a control block architecture. However, others, including the flight controller, as disclosed in the written description and drawings of the Dailey patent, do not include executable control blocks. Therefore, in view of the absence of a suggestion in the prior art to modify the Dailey flight controller to execute control blocks, the invention recited in claim 10, including a parameter defining a repetition period for executing the set of control blocks, cannot be obvious over the cited references. *In the event that this rejection is not withdrawn, Applicant requests identification of teachings in the prior art to make the modifications to Dailey that would render the claimed invention including a block processing cycle parameter.*

Applicant traverses the rejection of **claim 11** in **section 14** of the Office Action. Claim 11 depends from, and includes all the elements of, claim 10. Thus, for at least the reasons set forth above for claims 1 and 10, claim 11 is patentable over the prior art. Claim 11 recites a repetition cycle parameter specifying a period for restarting a cycle of the embedded control task. As mentioned previously herein above, the Dailey reference does not even disclose an embedded control task. Furthermore, the repetition cycle recited in McManus concerns a power calculation task. Thus, combining Dailey and McManus, at best, would render a periodic calculation of an output value according to a repetition period. Nowhere does the prior art suggest a parameter for designating the repetition period of the embedded control task comprising a multivariable linear program that supplied setpoints for controlling an industrial process. Finally, it is noted that the Office Action does not appear to distinguish between the control block execution period and the embedded task execution

period. The specification and claims make clear distinctions between these two periods and are not interchangeable. *In the event that this rejection is not withdrawn, Applicant specifically requests identification of prior art references teaching the specifically recited embedded control task repetition cycle parameter – which is distinguished, in both the claims and the specification, from the block processing cycle and specifies how often the embedded task is re-executed.*

Applicant traverses the rejection of **claims 12 and 24** in **section 15** of the Office Action. Claims 12 and 24 depend from, and include all the elements of, claims 11 and 13, respectively. Thus, for at least the reasons set forth above for claims 1, 10 and 11, claim 12 is also patentable, and claim 24 is patentable for at least the reasons set forth above with regard to claim 13. Claims 12 and 24 include the further specification that the embedded task repetition period exceeds the control block repetition period. The cited portions of the McManus patent neither disclose nor suggest these two distinct periods, and therefore cannot render claims 12 and 24 obvious. *Applicant specifically requests identification of the two distinct cycles as well as their relative durations/periods in the event that the rejection of this claim is not withdrawn.*

Applicant traverses the rejection of **claim 20** in **section 16** of the Office Action. Claim 20 depends from, and includes all the elements of, claim 13. Thus, for at least the reasons set forth above for claim 13, claim 20 is patentable. Claim 20 further specifies maintaining a repetition cycle parameter specifying a period for restarting a cycle of the embedded task. For at least the reasons set forth above regarding claim 8 (reciting a similar set of elements), claim 20 is also patentable.

Applicant traverses the rejection of **claim 21** in **section 17** of the Office Action. Claim 21 depends from, and includes all of the elements of, claim 20. Thus, for at least the reasons set forth above for claims 13 and 20, claim 21 is patentable. Claim 21 further specifies determining, by a supervisory control block, when a next repetition period of the embedded task is to commence based upon the repetition cycle parameter. For at least the

reasons set forth above regarding claim 9 (reciting a similar set of elements), claim 21 is also patentable.

Applicant traverses the rejection of **claim 22** in **section 18** of the Office Action. Claim 22 depends from, and includes all the elements of, claim 13. Thus, for at least the reasons set forth above for claim 13, claim 22 is patentable. Claim 22 further specifies a step of maintaining a block processing cycle parameter specifying a repetition period for commencing a cycle of processing the set of control blocks. For at least the reasons set forth above regarding claim 10 (reciting similar elements), claim 22 is patentable over the prior art.

Applicant traverses the rejection of **claim 23** in **section 19** of the Office Action for at least the reasons set forth above with regard to claim 20 (the previously rejected claim upon which the Office Action bases its rejection of claim 23). Applicant also traverses the rejection of claim 23 in view of the reasons set forth above with regard to claim 11 (including similar claim elements).

Applicant traverses the rejection of **claims 7 and 19** in **section 20** of the Office Action under Section 103(a) as obvious over Dailey in view of Daggett et al. and Westergren et al. U.S. Pat. No. 5,423,076. Claims 7 and 19 depend from, and include all the elements of, claims 5 and 17. Thus, for at least the reasons set forth above with regard to claims 1, 2, 5, 13, 14 and 17, claims 7 and 19 are patentable. Furthermore, while Westergren does indeed disclose a ratio block, there is no suggestion to place such a regulatory control block within the flight controller described in the Dailey reference. Neither Dailey nor Daggett et al. suggest a need to incorporate a ratio block into their specific examples of control systems. Westergren does not suggest that its ratio block is applicable in either the Dailey flight control system or the system disclosed in Daggett et al. *In the event that the rejection is not withdrawn, Applicant specifically requests identification of a motivation/suggestion in the prior art to modify the flight control system in Dailey to include the recited ratio control block.*

Applicant traverses the rejection, at section 21 of the Office Action, of claim 26 under Section 103(a) as obvious over Dailey U.S. Pat. No. 6,330,483 in view of Wright et al. U.S. Pat. No. 6,101,599. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not, in combination with Wright, render Applicant's claim 26 unpatentable since Dailey lacks a number of the recited elements.

The invention recited in claim 26 is directed to a multi-level multivariable industrial process control program execution framework for an industrial control processor. The recited *multi-level* control program execution framework thus includes at least two distinct levels of control program *execution*. A first cyclically executed sequence of instructions, executed at a relatively lower priority, is repeated according to a first *configurable* repetition period (e.g., every 5 seconds) to render setpoints for a process control variable (e.g., regulatory control blocks). In the illustrative embodiment of the invention, the first cyclically executed sequence of instructions, executed at a relatively lower priority, corresponds to the multivariable control application 138. The values (including setpoint values) rendered by the control application 138 (described as a linear program that operates upon potentially hundreds of input values) are generally computationally intensive, but generally less time-critical. The control processor executes the control application 138 after higher priority tasks have been executed by the control processor. Furthermore, the repetition cycle of the multivariable control application 138 is configurable – thus enabling a supervisor (e.g., a human, an automated supervisory monitor program, etc.) to adjust the repetition period according to needs/processing load.

The invention recited in claim 26 also includes a second cyclically executed sequence of instructions. The second cyclically executed sequence of instructions is executed at a higher execution priority level (e.g., as an interrupt-invoked foreground task) than the first cyclically executed instructions. The second cyclically executed sequence is repeated according to a second repetition period. In the illustrative embodiment, the second cyclically executed sequence includes the regulatory control blocks that carry out the interface between the control processor and the field devices that carry out the control instructions (e.g., setpoints) rendered by the multivariable control application 138. The regulatory control

blocks are executed after an interrupt is generated after a relatively short period of time (e.g., every half second) in comparison to the first repetition period of the multivariable control application. For at least the reasons expressed herein below, Applicant asserts that the invention recited in claim 26, including the first and second cyclically executed sequences of instructions, is neither disclosed nor suggested by the Dailey patent.

As previously explained, the Dailey patent, upon which the rejection of claim 26 is based, discloses a flight control system for a flying object (e.g., an airplane, rocket, missile, etc.). The Dailey patent discloses a control system including potentially multiple command channels – the output signals that control rudder, aileron, flap, etc. positions on the flying object. The Dailey patent first discloses a way for eliminating integrator windup (when a controlled element cannot change as quickly as desired by the control system). The Dailey patent also discloses a control method including assigning priorities to *output channel values* for controlling flight.

However, contrary to the Office Action's continued assertions, Dailey does not disclose carrying out control through *execution of the sequences of instructions* having differing priorities – as recited in claim 26. Instead, Dailey's reference to "priorities" concerns, as explained at col. 18, lines 22-41, control affecters. The primary control affecters are used first, then the secondary control affecters are used when the primary control affecters saturate. This teaching is reinforced at column 19, lines 46-64. Thus, Dailey discloses prioritization of control affecters (output channels) rather than prioritizing execution of the two distinct sets of cyclically executing program sequences described in claim 26. *The Office Action at section 23 continues to misconstrue the disclosure of the Dailey patent and erroneously concludes that the priorities recited in Dailey are somehow related to execution priority. As clearly/unequivocally disclosed in the Dailey reference itself – the priority, in the context of Dailey, relates to the manner in which previously calculated channel values are applied to control elements in the flying object. In the event that the rejection of claim 26 is not withdrawn, Applicant respectfully requests identification of explicit teaching within Dailey that the first and second priorities correspond to first and second execution precedence levels – as opposed to determining how the resulting channel values are applied in the flight control system.*

Dailey also appears to disclose only a single cyclically executed control loop that calculates both the primary and secondary channel values. Dailey, at col. 39, lines 1-3 refers to

beginning a new iteration cycle. Thus, at each iteration cycle, the controller calculates new values for all channels (both primary and secondary).

Dailey does not include a number of elements specifically recited in independent claim 26. As an initial matter, the Office Action does not identify any teaching within Dailey of a "first *configurable* repetition period." The Office Action cites disclosure of an iteration cycle (at col. 39, lines 1-3). However, the disclosure of "beginning a new iteration cycle" does not mean that a repetition period has been established (since the time to complete a single loop may change depending upon the amount of work performed during an iteration cycle) or that the duration of the repetition period is configurable. *In response to Applicant's previous remarks, the Office Action has now cited Wright as teaching a "configurable" cycle.* Applicant agrees that it is known to provide a configurable repetition period. However, there is no suggestion in Wright to provide a configurable repetition period for commencing a cycle for calculating setpoint values for process control variables.

Furthermore, there is no suggestion in Dailey to make such modification (i.e., adding a configurable repetition cycle time) to Dailey's disclosed control system. The control system cycle load in Dailey is not likely to change in view of its intended environment (i.e., a particular controlled flying object). Instead of being a general-purpose control system, Dailey discloses systems created specifically for a particular use (e.g., controlling a missile's flight path, an airplane's flight control surfaces, etc.). Thus, in the case of Dailey, a repetition period (if such fixed period even exists in Dailey) is established during programming of the control system and there is no suggestion in Dailey that the programmed repetition period is somehow changed through later configuration. In fact such changes might have a disastrous effect upon the stability of the system (contrary to the purpose of the invention – to improve the stability of the control system in response to large changes). There is therefore no incentive to provide a configurable repetition period in the Dailey flight control system.

Applicant previously stated that the Office Action did not identify the presence of distinct first *and* second cyclically executed sequences of instructions *as recited in claim 26*. The recited invention identifies two distinct cyclically *executed* instruction sequences operating at differing levels of priority and according to distinctly designated repetition periods. It is Applicant's understanding that Dailey discloses a single control sequence that is executed on a repeating basis to render values for the signal channels according to the L1 Optimization

Algorithm. *The Office Action states at paragraph 23 that the distinct first and second cyclically executed sequences correspond to execution of a first instruction at a first priority and a second instruction at a second priority.* Applicant submits that such analysis completely disregards a number of characteristics of the first and second sequences including, among other things: (1) they are *executed* at differing priorities, (2) they have distinct repetition cycles. Having clarified this request, Applicant requests that, in the event that the rejection of claim 26 is not withdrawn, any subsequent office action specifically identify the *distinct* first and second cyclically executed sequences of instructions that are executed at two distinct *execution* priority levels.

As previously explained, rather than identify two distinct execution levels in the Dailey patent, the Office Action references signal channels having differing (i.e., primary/secondary) priority levels that bear upon the manner in which the channel values are *applied* to flight control surface actuators. See, col. 18, lines 22-41 and col. 19, lines 46-64. The priority levels are assigned to the signal channels as part of optimizing control of the flying object. Primary channels are given higher importance than secondary channels during optimization. Nowhere does Dailey disclose or suggest that the signal channel values are rendered by program sequences that operate at differing execution priority levels based upon the priorities assigned to the output channels. Furthermore, since the channel values are calculated by a single control sequence, then there cannot be two distinctly designated control sequences.

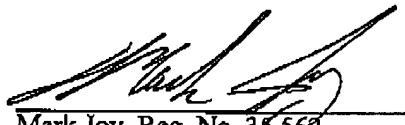
In addition to addressing the above shortcomings of Dailey's disclosure identified above, in the event that the rejection of claim 26 was not withdrawn, Applicant previously requested identification, within Dailey, of "a set of instructions for calculating a setpoint value for a process control variable" (in the first cyclically executed sequence of instructions). The Office Action references Dailey, at col. 15, lines 50-65 as disclosing such setpoint. However, nothing in Dailey suggests that the output variables identified in the equations are setpoint values. In the event that this rejection was not withdrawn, Applicant requested an explanation of how Dailey discloses a setpoint value for a process control variable at col. 15, lines 50-65. *Neither of these two requests have been addressed by the current Office Action.*

In re Appln. of Nick P. DiVittorio
Application No. 09/449,912

Conclusion

The application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



Mark Joy, Reg. No. 35,562
LEYDIG, VOIT & MAYER, LTD.
Two Prudential Plaza, Suite 4900
180 North Stetson
Chicago, Illinois 60601-6780
(312) 616-5600 (telephone)
(312) 616-5700 (facsimile)

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